What is claimed is:

1. A semiconductor memory device having an output driver in which a first NMOS transistor and a second NMOS transistor are connected in series, a drain of the first NMOS transistor is connected to an output pad, and the source of the second NMOS transistor is connected to a ground voltage, wherein:

a first internal voltage is applied to the gate of the first NMOS transistor and a second internal voltage is applied to the gate of the second NMOS transistor; and

a voltage level of the second internal voltage is lower than the voltage level of an external supply voltage.

2. The semiconductor memory device of claim 1, wherein the second internal voltage is generated directly from an internal voltage generating circuit of the semiconductor memory device or is externally applied.

3. The semiconductor memory device of claim 1, wherein the voltage level of the second internal voltage is different from the level of an operating voltage of the semiconductor memory device.

4. A semiconductor memory device having an output driver in which a first NMOS transistor and a second NMOS transistor are connected in series, the drain of the first NMOS transistor is connected to an output pad, and the source of the second NMOS transistor is connected to a ground voltage, having a driving circuit which applies a driving voltage to the gate of the second NMOS transistor in response to data, and an internal supply voltage, wherein a ground voltage level of the driving circuit is higher than the voltage level of the ground voltage to which the source of the second NMOS transistor is connected.

5. The semiconductor memory device of claim 4, wherein the voltage level of the driving voltage is different from the level of an operating voltage of the semiconductor memory device.

6. The semiconductor memory device of claim 4, wherein the voltage level of the driving voltage is lower than the voltage level of an external supply voltage.

7. A semiconductor memory device having an output driver in which a first NMOS tansistor and a second NMOS transistor are connected in series, the drain of the first NMOS transistor is connected to an output pad, and the source of the second NMOS transistor is connected to a ground voltage, and having a precharge transistor of which the source is connected to a connection node of the first NMOS transistor and the second NMOS transistor and of which drain is connected to a supply voltage, wherein the precharge transistor includes a voltage compensating circuit for lowering the rise in the voltage level of the connection node due to the rise in the voltage level of the gate of the first NMOS transistor.

8. The semiconductor memory device of claim 7, wherein the voltage compensating circuit comprises a capacitor which is connected between the gate and the source of the precharge transistor.

9. The semiconductor memory device of claim 8, wherein the capacitor has the same capacitance as a coupling capacitor between the gate and the source of the first NMOS transistor.

10. The semiconductor memory device of claim 7, wherein the precharge transistor is an NMOS transistor.